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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Federico Pio et al.
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For	:	IMPROVED FIELD-EFFECT TRANSISTOR AND CORRESPONDING MANUFACTURING METHOD

Examiner	:	Douglas A. Wille
Art Unit	:	2814
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Assistant Commissioner for Patents
Washington, DC 20231

RULE 131 DECLARATION

Assistant Commissioner for Patents:

I, Federico Pio, residing at Via Volturno Fontana, 80, I-20047 Brugherio, Italy, declare as follows:

I am an original, first, and joint inventor of the subject matter which is claimed and for which a patent is sought for the application identified above.

I was in possession of the invention defined by the claims of the application identified above ("the present application") prior to June 24, 1998. Attached as Appendices I, II, and IV are internal reports of STMicrolectronics, the assignee of the present application, regarding:

the mask set (named ZZ33) in which a structure was realized according to the process recited in the claims of the present application;

the "merging programs" used to generate automatically the photo-masks involved in the realization of the structure; and

the process flow (named CMOSF6X) used to produce the structure in a CMOS process for Single-Poly or Doubly-Poly Flotox-EEPROMs.

Attached as Appendix III is a document that includes layout views of the ZZ33 mask set.

As can be appreciated from the dates of the reports and the layout views document, the preliminary idea was conceived and realized in 1997 in the mask set ZZ33 and was realized on silicon and characterized in late 1997 and early 1998 prior to June 24, 1998.

In the following is a more detailed description of the attached documentation.

January 1998 Report entitled F6X Process Flow (Appendix I)

This document contains the complete flow of the CMOSF6X process. The important points are the ones related to the P-well implant mask (055; this mask can also be referred to as "NoTub"), see page 4. The mask 055 protects all N-well regions and all active area regions within the NoTub drawing layer (see Appendix II, page 6), so that the corresponding channel region of a transistor is doped with the substrate concentration in the central portion and a higher P-type concentration in the edge portion because of the lateral diffusion of the near-by P-well implant. The P-well drive-in, and therefore also the corresponding lateral diffusion is mainly obtained during the HV/LV gate and tunnel oxide thermal growths (performed at 800C/750C and 900C+1000C annealing, respectively, see pages 6-7 of Appendix I), but also during all subsequent thermal treatments, even if with less efficiency.

May 1998 Report entitled ZZ33 Test Pattern Description (Appendix II)

This report contains the description of the test structures in the mask set ZZ33 after a partial mask set modification (as is evident in Appendix III, the mask set was originally generated during 1997) following preliminary characterization of first silicon; the most relevant parts are:

the merging flow (dated April 14th 1998), pag.6/77; and

the description of TEGs (more specifically the ones including the NoTub transistor structures, i.e. see TEGs 6, 10, 8, 12, 15, 19 and 20, respectively at pp.13, 17, 15, 19, 22, 26 and 27, including different transistor options and different geometries, as well as

some Flotox-EEPROM cells implementing the proposed solution in the byte switch, i.e. TEG SP06, p. 39/77)

The use of merging flow deserves some explanations: in the table at p. 6/77 are reported: the mask number (also imprinted on the silicon, col.1), the field (D=dark, C=clear, col.2), the mask name (for ease of reference, col.3), the merging program used to generate the pattern (with Boolean operations and sizing between the drawing layers, col.4) and the eventual final sizing in the mask generation (col.5).

In most of the drawing layers, the geometries produced on the photo-mask are exactly as they are drawn (i.e. mask 015 = Nwell is obtained from the geometries drawn on layer 1 without any additional operation nor sizing; mask 505 = Poly is drawn on layer 13 as it is desired, similarly for 800 = Metal1, 850 = Vias1, 860 = Metal2, 870 = Vias2, 880 = Metal3, whose geometries exactly correspond to the layout on layers 23, 25, 27, 32 and 34, respectively).

On the contrary, for some other masks it is more convenient to use an automatic data treatment in the photo-mask generation; this is the case of mask 105 = Active Area, for which the (known and reproducible) dimensional variations produced by the process are compensated at mask level: during field oxidation for the recessed LOCOS isolation (see flusf6x2.pdf, pagg.2-3) a bird's beak is grown under the nitride layer, therefore a decrease of final dimension is produced, with respect to the nitride regions patterned with photo-mask 105. It is clear that, on the other hand, it would be highly desirable that the database corresponds to the target values (i.e. a drawn geometry of 1.0μm for a transistor width of 1.0μm.). To achieve both results a sizing is applied in the photo-mask generation; for Active Area mask 105 all geometries drawn on layer 2 exactly as desired on silicon are grown by 0.25μm by side (col.5) in the photo-mask generation, in order to compensate the dimensional loss in process due to bird's beak formation during Recessed LOCOS isolation.

For other masks, it is possible to minimize the effort (and corresponding potential source of errors) if the final geometry to be patterned on the photo-mask can be obtained by a pre-defined set of (Boolean) operations on selected drawing layers, including eventual intermediate sizing.

This is the case of the involved mask 055 = NoTub (or P-well); I explain the merging program for this mask: it is clear that the P-well implant must be avoided on any N-well region (mask 015, drawn on layer 1).

In our embodiment of the invention we also want to avoid the P-well implant on selected active area regions (drawn on layer 2) where the NoTub transistors are realized: since not all active area regions must be protected from the implant, an "identification" layer (number 3) is used to surround only the interested regions. Therefore the Boolean operation (2 AND 3) selects ONLY the Active Area regions of the NoTub type. In our embodiment of the invention we propose that a distance is kept between the edge of active area and the NoTub/P-well implant mask; this is achieved by the +0.6μm Oversize applied to the identified regions: [(2 AND 3) OV +0.6].

Finally the obtained geometries are added (OR) to the N-well regions drawn on layer 1, to obtain: [(2 AND 3) OV +0.6] OR 1.

It can be noted that, since photo-mask 105 Active Area had a final sizing of +0.25μm, the true spacing between the 105 regions (defining the nitride layer) and the 055 NoTub regions (protecting from the P-well implant) is reduced to 0.35μm since both are enlargements (+0..25μm and +0.6μm, resulting in 0.6μm – 0.25μm) from the active area geometries drawn on the database.

ZZ33 Mask Set: Full Layout (Appendix III)

This document contains some layout views of the ZZ33 mask set (see also Appendix II, fig.1 p.7; with respect to it, the layout is rotated by 90 degrees clock-wise).

Pages 1 to 5 are subsequent enlargements (starting from the global view) finally showing the region where the mask names and revisions, the logo and fabrication year (1997) are printed on silicon.

Pages 6-10 show progressive enlargements of the layout in order to show a TEG including several geometries featuring different spacing between the NoTub mask 055 and the Active Area mask 105; these structures correspond to embodiments of the invention.

Pages 11-18 are progressive enlargements (starting from the global view) showing the layout of one HV NoTub transistor as described in the invention. Note that layer 3 "NoTub" (orange diagonal stripes) surrounds large regions of the TEGs, including several active areas and therefore several transistor structures. According to an original merging

program, the whole region would have been protected from the P-well implant. On the contrary, with the modified merging program only small regions around each transistor will be protected by the P-well implant, with 0.35μm overlap on the final nitride patterns defined by mask 105.

Pages 19 to 21 show the layout of different geometries and of LV NoTub transistors, also present in the ZZ33 mask set.

Pages 22 and 23 show the use of a NoTub transistor in an array of Single-Poly EEPROM cells, as control-gate byte switch. Also this structure is present in the ZZ33mask set.

December 11, 1997 Report (Appendix IV)

As is clear from the issuance date of this document, the preliminary results on silicon processed with the ZZ33 mask set (including the NoTub transistors object of the invention) were already available in 1997 (see introduction, p.2).

The silicon characterized in this report was processed according to the original flow.

By comparing tables 1 and 3, and 2 and 4 (pagg 4-5), it can be seen the impact on threshold voltage of the NoTub mask on otherwise equivalent HV transistors: DVT of about 0.3V and 0.6V was measured on LVS and native transistors, respectively. Other electrical parameters are compared in table 11, p.9.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

September 16th 2003

Date

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